REMARKS

Claim Objections

The Examiner objected to claims 4-8, 10, 11, 13, and 18-21. Applicants have amended claims 4-8, 10, 11, 13, and 18-21 so as to make clear that the swapped, current context is associated with the first thread as recited in claims 1 and 15, from which claims 4-8, 10, 11, 13, and 18-21 depend. Accordingly, the objection should be withdrawn.

35 U.S.C. § 112

The Examiner rejected claims 11 and 12 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. The Applicants have addressed the points made by the examiner in the objections to claims 11 and 12 *supra*. Accordingly, the rejection should be withdrawn.

35 U.S.C. § 102

The Examiner rejected claims 1, 12, 14-16, 21, 24, and 26 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,212,544 ("Borkenhagen").

Claim 1 recites "[a] method of operating a multithreaded parallel processor comprising… directing the processor having a plurality of microengines, a microengine having a context event arbiter, to swap, based on a user-specified parameter specified in a context-swap instruction, a currently running context, corresponding to a first thread, in a specified microengine to let another context, corresponding to a different thread that is ready to execute, execute in that microengine…"

The examiner contends that **"Borkenhagen teaches: A method of operating a multithreaded parallel processor comprising…directing the processor having a plurality of microengines (Figure 3) to swap…"**[1]

Applicant reproduces Figure 3 from Borkenhagen below:

[1] Office Action, Mail Date April 27, 2009, Page 5

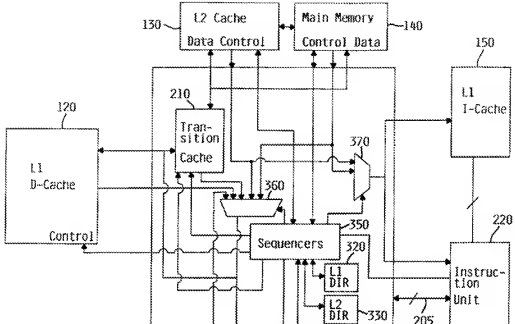

FIGURE 3

The examiner does not state which elements of Figure 3 in Borkenhagen correspond to microengines as recited in claim 1. Assume *arguendo* that the microengines recited in claim 1 correspond to the execution units 260, 270, 280 in Figure 3. These execution units are reserved for various tasks in Borkenhagen:

> **Instructions from the L1 I-cache 150 are preferably output to an instruction unit 220 which…controls the execution of multiple threads by the various subprocessor units, e.g., branch unit 260, fixed point unit 270, storage control unit 200, and floating point unit 280 and others as specified by the architecture of the data processing system 10.**[2]

It is not clear from the passage cited *supra* whether the threads are associated with each subprocessor unit, or whether they are simply executed upon by the subprocessor units, and are,

[2] Borkenhagen, Column 8, Lines 47-54

rather, associated with a single processor. In fact, the threads in Borkenhagen are simply executed by a single processor:

> **[A]nother technique to improve the efficiency of hardware within the CPU is to divide a processing task into independently executable sequences of instructions called threads. This technique is related to breaking a larger task into smaller tasks for independent execution by different processors except *here the threads are to be executed by the same processor.*[3]**

It is clear from the passages cited *supra* and Figure 3 of Borkenhagen that the architecture of the system described and/or suggested by Borkenhagen do not suggest the foregoing features of claim 1 :

> **The storage control unit 200, the execution units 260, 270, and 280 and the instruction unit 220 are all operationally connected to the thread switch logic 400 which determines which thread to execute.[4]**

That is, even if the execution units 260, 270, and 280 could be conceived as microengines, which Applicant does not concede, the execution units do not possess separate context event arbiters, and as a consequence does not suggest the features of: "to swap based on a user-specified parameter specified in a context-swap instruction, a currently running context, corresponding to a first thread, in a specified microengine to let another context, corresponding to a different thread that is ready to execute," as recited in claim 1.

Borkenhagen, thus neither describes nor suggests "[a] method of operating a multithreaded parallel processor comprising… directing the processor having a plurality of microengines, a microengine having a context event arbiter, to swap, based on a user-specified parameter specified in a context-swap instruction, a currently running context, corresponding to a first thread, in a specified microengine to let another context, corresponding to a different thread that is ready to execute, execute in that microengine…," as recited in claim 1.

Claims 15 and 24 recite similar features as recited in claim 1. Accordingly, the rejection should be withdrawn.

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[3] Borkenhagen, Column 3, Lines 59-65, *emphasis* added
[4] Id., Column 9, Lines 22-25

35 U.S.C. § 103

The Examiner rejected claims 4-8, 10, 11 13, 18-20, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Borkenhagen in view of Official Notice.

Claim 22 recites similar features as recited in claim 1. Claims 4-8, 10, 11 13, and 18-20 depend from claims 1 and 15. Borkenhagen was shown *supra* to neither describe nor suggest all of the features of claims 1 and 15. Furthermore, even if examiner's Official Notice were acceptable to the Applicants as a prior art reference for a register stack[5], such Official Notice neither describes nor suggests "[a] method of operating a multithreaded parallel processor comprising... directing the processor having a plurality of microengines, a microengine having a context event arbiter, to swap, based on a user-specified parameter specified in a context-swap instruction, a currently running context, corresponding to a first thread, in a specified microengine to let another context, corresponding to a different thread that is ready to execute, execute in that microengine...," as recited in claim 1.

Borkenhagen and Official Notice, alone or in combination, neither describe nor suggest "[a] method of operating a multithreaded parallel processor comprising... directing the processor having a plurality of microengines, a microengine having a context event arbiter, to swap, based on a user-specified parameter specified in a context-swap instruction, a currently running context, corresponding to a first thread, in a specified microengine to let another context, corresponding to a different thread that is ready to execute, execute in that microengine...," as recited in claim 1, and similarly in claims 15 and 22. Accordingly, the rejection should be withdrawn.

In view of the foregoing, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner's earliest convenience.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

[5] Applicants do not conced that this is the case.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any deposits or fees to account no. 06-0150, referencing attorney docket number 10559-0303US1.

Respectfully submitted,

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